S-BAND SYNTHESIZER OF FREQUENCIES AND WIDEBAND LFM SIGNALS

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Summary

In the article is considered the S-band synthesizer of frequencies and wideband LFM signals, which is constructed on the basis of LFM signal digital way forming on a video frequency with usage of high-speed field programmable gate array (FPGA), chips of read-only memory and random-access memory (ROM and RAM), digital-analog converters (DAC), quadrature one-band modulator and frequency multipliers of signal. The synthesizer provides the interpulse capability of the changing of LFM oscillations velocity and initial phase signal, pulse durations with LFM and deviation value. Are shown the synthesizer structure diagram, the results of experimental researches of its output signals, the synthesizer design features and its reliability evaluation.

Key words:
The direct digital synthesizer (DDS), linear frequency modulation (LFM).

Introduction

Now in the radars of different assignment the signals synthesis digital devices are widely used. They allow not only to synthesize the requirement types of signals with necessary accuracy and to change their parameters (frequency deviation (W_C), duration (t_C), frequency velocity changing sign and initial phase), but also to put in them the preemphasis for declinations compensation from the given laws of modulation, which are necessarily brought by amplifying-transforming tract of the radar transmitter.

The requirements raised to permissible signal variations from given laws of modulation, are determined by the way of processing, adopted in the radars, by the character of these variations and with increase of signal basis $D = t_C \cdot W_C$ are increased [1].

Brief review

Practically in the radars are applied three types of digital devices of frequencies and signals synthesis:

1. The direct digital synthesizers (DDS), in which at first with frequency of clocking ($f_т$) are evaluated the signal phase codes, which then are converted to readout codes of synthesized oscillations values. The circuitry basis of such DDS are constituted by digital multi-stage accumulators (AC) and functional converters (FC), as arithmetic-logic and (or) storage devices [1 - 5].
2. DDS, operating similar synthesis algorithm, but built on the basis of digital signal processors (DSP), which power and response recently have considerably increased [6, 7], that makes such DDS rather perspective.
3. The digital synthesizers, in which from ROM or RAM are selected beforehand calculated for clock periods of time and written to them codes of readout values of synthesized oscillations.

The transformation of numerical codes of readout values to analog form in all types of synthesizers is implemented with the help of DAC, low-pass filters (LPF) or band-pass filters (BPF).

The widespread of DDS of the first and second type while is restrained by relative inaccessibility and specially by the remedies cost for the development and debugging of the devices on their basis. The synthesizers of the third type are more simple devices, have

the best spectral characteristics, do not require the complicated and expensive remedies for the development and debugging and at usage accessible, high-speed and relatively cheap modern element basis, consisted of a DAC, ROM, RAM and FPGA [8 - 11], are currently preferable.

Results

Usually in the particular radar are used small suite of signals, which can beforehand be calculated with necessary accuracy and be written to relatively slow ROM, and then, during a space between radiated pulses, any of them is copied in fast RAM, made as separate chips or is included in FPGA structure. During the next starting pulse, the signal, red out from RAM, converted in the analogue form and transferred in given frequency band, goes at the output of the synthesizer. In the ROM can be written the necessary quantity of harmonic sine-wave oscillations, which are used for taking out of amplitude-frequency (AFC) and phase-frequency characteristics (PFC) of separate devices or the radar transmitter the whole with the purpose of detection of variations from the demanded to them requirements. For obtaining the maximum possible frequency deviation at the output of the synthesizer at the limited high-speed of digital devices, included in it, the signal is usually synthesized on video frequency in the quadrature (sin and cos), and then with the help of the one-band modulator (OM), frequency multipliers or mixers is transferred to given frequency band.

The structure diagram of the synthesizer, designed with the accordance of abovementioned, is shown in fig. 1.

Except of the mentioned devices are envisaged the electronic switches (ES), ensuring the necessary suppression of signals ″diving″ in the space between radiated pulses, and the chip of IC configuration FPGA (ICF), permits to create in it the different schemes of digital devices, including the AC and FC schemes.

Selection of clock rate values ($f_т$), of high-speed FPGA, ROM volumes (C_{ROM}) and RAM (C_{RAM}), digital capacity of the DAC and sample quantity (N) of the signal are

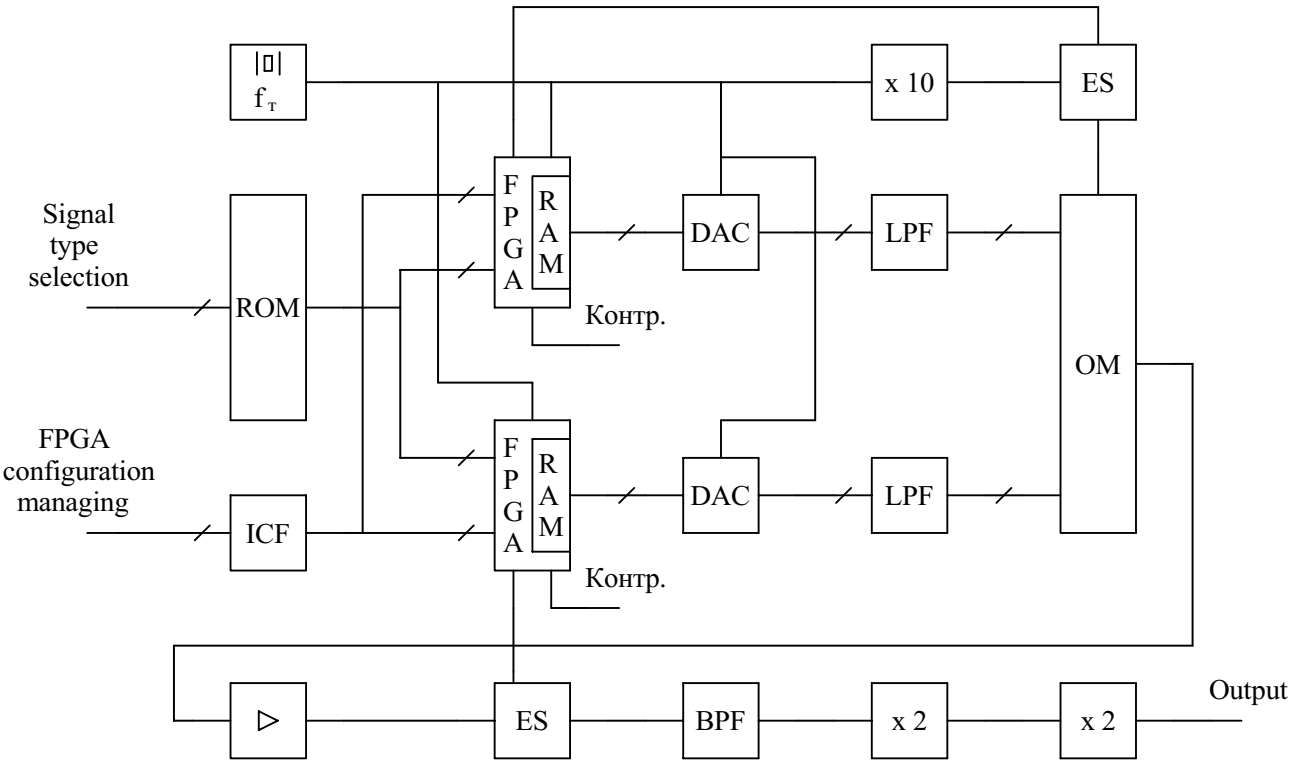

Fig. 1
Structure diagram of the synthesizer

determined by given requirements to the signal parameters and its spectrum, and also to permissible relative mean square declinations ε(t), which can be evaluated using simple ratios received for synthesizers of frequencies [2] and signals [12]:

$$Q_{na} = -6 \cdot p_a - 1.8 \text{ [dB]} \quad (1)$$

$$Q_{n\varphi} = -6 \cdot p_\varphi + 8.1 \text{ [dB]} \quad (2)$$

$$f_. \geq (2.5 - 3) \cdot f_{Wmax} \quad (3)$$

$$C_{RAM} = 0.5 \cdot t_W \cdot f_. \cdot p_a \quad (4)$$

$$C_{ROM} = K \cdot C_{RAM} \quad (5)$$

$$\varepsilon(t) = \pi/6 \cdot (W_C/N) \quad (6),$$

where:

Q_{na}, $Q_{n\varphi}$ - relations of quantization noises power of amplitude in DAC and noises of phase discretization in the band of the restoring filter (LPF) according to power of useful signal;

p_a, p_φ - the quantity of the DAC stages and the quantity of the stages, used for reversion to FC accordingly;

$f_{c\ max}$ - maximum LFM frequency of video signal;

K - quantity of the signals in the suite.

It is necessary to note, that the formulas (1), (2) don't account the influences on the spectrum of ″glitch″ signal, existing in DAC and the increase of the level of the spurious components in the signal spectrum at frequency approximation to $f_{c\ max}$, which can be about 10 dB [2, 13].

In this synthesizer working with $f_. \approx 80$ MHz are used the reprogrammable ROM of TB28F400 type, FPGA of EPF10K30E type, FPGA configuration scheme of EPC2 type, DAC of AD9731R type, quadrature modulator of U2790B type, Butterwort LPF of the 7-th order, amplifiers of ERA5SM type and frequency multipliers on the transistors of 2T647A-2 type.

The synthesizer provides changing of LFM pulses duration within the limits of 5 - 20 μs, frequency deviation up to 200 MHz, initial Cтase (0, π) and velocity cтanging sign in each pulse of the radar transmitter irradiation, and also provides the operation in continuous mode (without changing of the signal parameters) with LFM or in frequency synthesis mode with the step ~1 MHz.

Chosen element base and designed construction allow to work with higher (~120MHz) clock frequency.

The special attention was given to developing and experimental drill of frequency multipliers of the signal with LFM. Input LPF and the output Butterwort BPF for frequency multipliers were calculated with the accounting of experimentally received input and output impedances of the transistor in operation mode at input power of 15-20 mWt. AFC and PFC declinations in the band ±100 MHz from average value of the output signal frequency in S-band have composed no more than ± 0.6 dB and ± 5^0 accordingly. Frequency multipliers PFC were measured with the help of the installation including a self-excited oscillator, working in mode of dividing on 2 or 4 of clocking frequency and phase meter of ″ФК2-33″ type.

The main experimental results for one of operational modes of the synthesizer are shown in fig. 2 - 4.

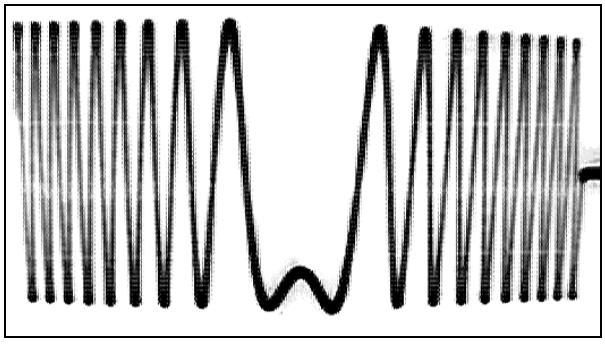

Fig. 2. W_C=7.5 MHz, t_C=10 μs

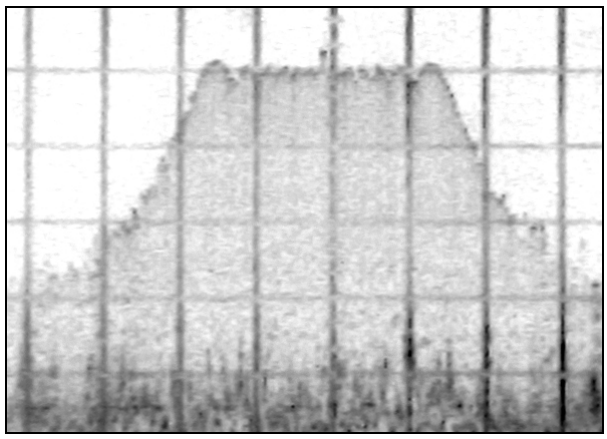

Fig. 3. W_C=7.5 MHz, t_C=10 μs

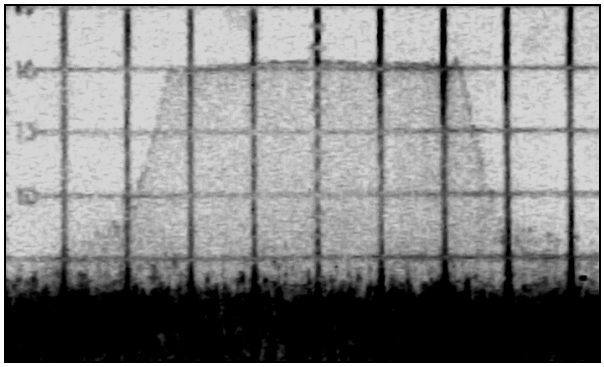

Fig. 4. W_C=50 MHz, t_C=10 μs

Rather small declinations of LFM signal real spectrum from theoretically calculated allow to hope for obtaining of a side-lobe level (SL) of compressed LFM signal no more then - (25 - 30) dB [2, 14]. The results of experimental testing of SL drilled signals of the synthesizer and transmitter of the radar, and also the influence on them of used kind of preemphasis is expected to publish later.

The synthesizer is constructed as two functionally and structurally independent units, in which one the digital devices are located, and in the other – the analogue devices, that improve their electromagnetic compatibility. The synthesizer consists of the devices, which form the heterodyne ultra high frequency oscillations, the oscillations of intermediate frequency and necessary pulse oscillations for radar transmitter control and system of digital processing of the received signals. With the purpose of the operating reliability each of the units are reserved and ensures the operation of both basic, and stand-by units, thus the rate of probability of trouble-free operation consists 0.998 for 3000 hours of operation. Synthesizer consumption is 19 Wt.

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